## LV8712T / LV8713T

## Bi-CMOS LSI

## PWM Constant-Current Control Stepping Motor Driver

## Overview

The LV8712T and LV8713T are microstepping motor drivers with built-in translator for easy operation. The LV8712T supports full-step, half-step, quarter-step, and $1 / 8$-step resolution. The LV8713T supports full-step, half-step, $1 / 16$-step, and $1 / 32$-step resolution. These ICs are optimal for driving stepping motor of scanner and small printer.

## Features

- Single-channel PWM constant-current control stepping motor driver incorporated.
- Microstepping is configurable to the following modes:

Full-step, half-step, quarter-step, or $1 / 8$-step. (LV8712T)
Full-step, half-step, $1 / 16$-step, or $1 / 32$-step. (LV8713T)

- CLK-IN input facilitates the control of microstepping.
- Power-supply voltage of motor $: \mathrm{VM} \max =18 \mathrm{~V}$
- Output current
- Output ON resistance $\quad:$ RON $=1.1 \Omega$ (upper and lower total, typical, $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )
- Thermal shutdown circuit and low voltage detecting circuit incorporated.


## Typical Applications

- POS Printer
- Scanner
- Thermal Printer Unit
- Security camera
- Air-conditioner


## Selection Guide

| Part Number | Microstepping mode |
| :---: | :---: |
| LV8712T | Full-,half-,quarter-,1/8-step |
| LV8713T | Full-,half-,1/16-,1/32-step |

## Pin Assignment



## Package Dimension

unit: mm (typ)
3260A


Mounting Pad Sketch


| (Unit:mm) |  |
| :---: | :---: |
| Reference symbol | TSSOP24 (225mil) |
| eE | 5.80 |
| e | 0.50 |
| b3 | 0.32 |
| I1 | 1.00 |

Caution: The package dimension is a reference value, which is not a guaranteed value.

## Block Diagram



LV8712T/LV8713T

## Specifications

## Absolute Maximum Ratings at $\mathbf{T a}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Motor supply voltage | VM max |  | 18 | V |
| Logic supply voltage | $\mathrm{V}_{\text {CC }}$ max |  | 6 | V |
| Output peak current | lo peak | Each 1ch, tw $\leq 10 \mathrm{~ms}$, duty $20 \%$ | 1.0 | A |
| Output continuousness current | $\mathrm{I}_{0}$ max | Each 1ch | 800 | mA |
| Logic input voltage | $\mathrm{V}_{\text {IN }}$ |  | -0.3 to $V_{C C}+0.3$ | V |
| Allowable power dissipation | Pd max | * | 1.35 | W |
| Operating temperature | Topr |  | -20 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tstg |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

* Specified circuit board: $57.0 \mathrm{~mm} \times 57.0 \mathrm{~mm} \times 1.7 \mathrm{~mm}$, glass epoxy 2-layer board.


## Allowable Operating Ratings at $\mathbf{T a}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$

| Parameter | Symbol | Conditions | Ratings | 4 to 16 |
| :--- | :--- | :--- | ---: | :---: |
| Motor supply voltage range | VM |  | V |  |
| Logic supply voltage range | $\mathrm{V}_{\mathrm{CC}}$ |  | 2.7 to 5.5 | V |
| Logic input voltage | $\mathrm{V}_{\text {IN }}$ |  | -0.3 to $\mathrm{V}_{\mathrm{CC}}+0.3$ | V |
| VREF input voltage range | VREF |  | 0 to $\mathrm{V}_{\mathrm{CC}}-1.8$ | V |

Electrical Characteristics at $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VM}=12 \mathrm{~V}, \mathrm{VCC}=3.3 \mathrm{~V}, \mathrm{VREF}=1.0 \mathrm{~V}$

| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| Standby mode current drain | IMstn | PS = "L", no load |  |  | 1 | $\mu \mathrm{A}$ |
|  | ${ }^{\text {I CCstn }}$ | PS = "L", no load |  |  | 1 | $\mu \mathrm{A}$ |
| Operating mode current drain | IM | PS = "H", no load | 0.3 | 0.5 | 0.7 | mA |
|  | ICC | PS = "H", no load | 0.9 | 1.3 | 1.7 | mA |
| Thermal shutdown temperature | TSD | Design guarantee |  | 180 |  | ${ }^{\circ} \mathrm{C}$ |
| Thermal hysteresis width | $\Delta T S D$ | Design guarantee |  | 40 |  | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {CC }}$ low voltage cutting voltage | VthV ${ }_{\text {CC }}$ |  | 2.1 | 2.4 | 2.7 | V |
| Low voltage hysteresis voltage | VthHIS |  | 100 | 130 | 160 | mV |
| REG5 output voltage | Vreg5 | $\mathrm{I}^{\mathrm{O}}=-1 \mathrm{~mA}$ | 4.5 | 5 | 5.5 | V |
| Output on resistance | RonU | $\mathrm{I}^{\mathrm{O}}=-800 \mathrm{~mA}$, Source-side on resistance |  | 0.78 | 1.0 | $\Omega$ |
|  | RonD | $\mathrm{l} \mathrm{O}=800 \mathrm{~mA}$, Sink-side on resistance |  | 0.32 | 0.43 | $\Omega$ |
| Output leakage current | Ioleak | $\mathrm{V}_{\mathrm{O}}=15 \mathrm{~V}$ |  |  | 10 | $\mu \mathrm{A}$ |
| Diode forward voltage | VD | ID $=-800 \mathrm{~mA}$ |  | 1.0 | 1.2 | V |
| Logic pin input current | $\mathrm{I}_{1} \mathrm{~N}^{\text {L }}$ | $\mathrm{V}_{\text {IN }}=0.8 \mathrm{~V}$ | 4 | 8 | 12 | $\mu \mathrm{A}$ |
|  | ${ }_{1 \times}{ }^{H}$ | $\mathrm{V}_{\mathrm{IN}}=3.3 \mathrm{~V}$ | 22 | 33 | 45 | $\mu \mathrm{A}$ |
| Logic high-level input voltage | $\mathrm{V}_{1 N \mathrm{H}}$ |  | 2.0 |  |  | V |
| Logic low-level input voltage | $\mathrm{V}_{\text {IN }} \mathrm{L}$ |  |  |  | 0.8 | V |
| VREF input current | IREF | $\mathrm{VREF}=1.0 \mathrm{~V}$ | -0.5 |  |  | $\mu \mathrm{A}$ |
| Current setting comparator threshold voltage (current attenuation rate switching) | Vtatt00 | ATT1 $=\mathrm{L}, \mathrm{ATT} 2=\mathrm{L}$ | 0.191 | 0.200 | 0.209 | V |
|  | Vtatt01 | ATT1 $=\mathrm{H}, \mathrm{ATT} 2=\mathrm{L}$ | 0.152 | 0.160 | 0.168 | V |
|  | Vtatt10 | ATT1 $=\mathrm{L}, \mathrm{ATT} 2=\mathrm{H}$ | 0.112 | 0.120 | 0.128 | V |
|  | Vtatt11 | ATT1 $=$ H, ATT2 $=\mathrm{H}$ | 0.072 | 0.080 | 0.088 | V |
| Chopping frequency | Fchop | Cchop $=220 \mathrm{pF}$ | 36 | 45 | 54 | kHz |
| CHOP pin threshold voltage | $\mathrm{V}_{\mathrm{CHOP}} \mathrm{H}$ |  | 0.6 | 0.7 | 0.8 | V |
|  | $\mathrm{V}_{\mathrm{CHOPL}}$ |  | 0.17 | 0.2 | 0.23 | V |
| CHOP pin charge/discharge current | Ichop |  | 7 | 10 | 13 | $\mu \mathrm{A}$ |
| MONI pin saturation voltage | Vsatmon | Imoni $=1 \mathrm{~mA}$ |  | 250 | 400 | mV |

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Continued from preceding page

| Parameter |  | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | min |  | typ | max |  |
| Current setting comparator threshold voltage (current step switching) | 8W1-2-phase drive <br> (1/32-step at LV8713T) |  | Vtdac0_2W | Step 0 (When initialized: channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |
|  |  | Vtdac1_8W | Step 1 (Initial state+1) | 0.191 | 0.200 | 0.209 | V |
|  |  | Vtdac2_8W | Step 2 (Initial state+2) | 0.191 | 0.200 | 0.209 | V |
|  |  | Vtdac3_8W | Step 3 (Initial state+3) | 0.189 | 0.198 | 0.207 | V |
|  |  | Vtdac4_8W | Step 4 (Initial state+4) | 0.187 | 0.196 | 0.205 | V |
|  |  | Vtdac5_8W | Step 5 (Initial state+5) | 0.185 | 0.194 | 0.203 | V |
|  |  | Vtdac6_8W | Step 6 (Initial state+6) | 0.183 | 0.192 | 0.201 | V |
|  |  | Vtdac7_8W | Step 7 (Initial state+7) | 0.179 | 0.188 | 0.197 | V |
|  |  | Vtdac8_8W | Step 8 (Initial state+8) | 0.175 | 0.184 | 0.193 | V |
|  |  | Vtdac9_8W | Step 9 (Initial state+9) | 0.171 | 0.180 | 0.189 | V |
|  |  | Vtdac10_8W | Step 10 (Initial state+10) | 0.167 | 0.176 | 0.185 | V |
|  |  | Vtdac11_8W | Step 11 (Initial state+11) | 0.163 | 0.172 | 0.181 | V |
|  |  | Vtdac12_8W | Step 12 (Initial state+12) | 0.158 | 0.166 | 0.174 | V |
|  |  | Vtdac13_8W | Step 13 (Initial state+13) | 0.152 | 0.160 | 0.168 | V |
|  |  | Vtdac14_8W | Step 14 (Initial state+14) | 0.146 | 0.154 | 0.162 | V |
|  |  | Vtdac15_8W | Step 15 (Initial state+15) | 0.140 | 0.148 | 0.156 | V |
|  |  | Vtdac16_8W | Step 16 (Initial state+16) | 0.132 | 0.140 | 0.148 | V |
|  |  | Vtdac17_8W | Step 17 (Initial state+17) | 0.126 | 0.134 | 0.142 | V |
|  |  | Vtdac18_8W | Step 18 (Initial state+18) | 0.118 | 0.126 | 0.134 | V |
|  |  | Vtdac19_8W | Step 19 (Initial state+19) | 0.112 | 0.120 | 0.128 | V |
|  |  | Vtdac20_8W | Step 20 (Initial state+20) | 0.102 | 0.110 | 0.118 | V |
|  |  | Vtdac21_8W | Step 21 (Initial state+21) | 0.094 | 0.102 | 0.110 | V |
|  |  | Vtdac22_8W | Step 22 (Initial state+22) | 0.086 | 0.094 | 0.102 | V |
|  |  | Vtdac23_8W | Step 23 (Initial state+23) | 0.078 | 0.086 | 0.094 | V |
|  |  | Vtdac24_8W | Step 24 (Initial state+24) | 0.068 | 0.076 | 0.084 | V |
|  |  | Vtdac25_8W | Step 25 (Initial state+25) | 0.060 | 0.068 | 0.076 | V |
|  |  | Vtdac26_8W | Step 26 (Initial state+26) | 0.050 | 0.058 | 0.066 | V |
|  |  | Vtdac27_8W | Step 27 (Initial state+27) | 0.040 | 0.048 | 0.056 | V |
|  |  | Vtdac28_8W | Step 28 (Initial state+28) | 0.032 | 0.040 | 0.048 | V |
|  |  | Vtdac29_8W | Step 29 (Initial state+29) | 0.022 | 0.030 | 0.038 | V |
|  |  | Vtdac30_8W | Step 30 (Initial state+30) | 0.012 | 0.020 | 0.028 | V |
|  |  | Vtdac31_8W | Step 31 (Initial state+31) | 0.002 | 0.010 | 0.018 | V |
|  | 4W1-2-phase <br> drive <br> (1/16-step <br> at LV8713T) | Vtdac0_4W | Step 0 (When initialized: channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |
|  |  | Vtdac2_4W | Step 2 (Initial state+1) | 0.191 | 0.200 | 0.209 | V |
|  |  | Vtdac4_4W | Step 4 (Initial state+2) | 0.187 | 0.196 | 0.205 | V |
|  |  | Vtdac6_4W | Step 6 (Initial state+3) | 0.183 | 0.192 | 0.201 | V |
|  |  | Vtdac8_4W | Step 8 (Initial state+4) | 0.175 | 0.184 | 0.193 | V |
|  |  | Vtdac10_4W | Step 10 (Initial state +5 ) | 0.167 | 0.176 | 0.185 | V |
|  |  | Vtdac12_4W | Step 12 (Initial state+6) | 0.158 | 0.166 | 0.174 | V |
|  |  | Vtdac14_4W | Step 14 (Initial state+7) | 0.146 | 0.154 | 0.162 | V |
|  |  | Vtdac16_4W | Step 16 (Initial state+8) | 0.132 | 0.140 | 0.148 | V |
|  |  | Vtdac18_4W | Step 18 (Initial state +9 ) | 0.118 | 0.126 | 0.134 | V |
|  |  | Vtdac20_4W | Step 20 (Initial state+10) | 0.102 | 0.110 | 0.118 | V |
|  |  | Vtdac22_4W | Step 22 (Initial state+11) | 0.086 | 0.094 | 0.102 | V |
|  |  | Vtdac24_4W | Step 24 (Initial state+12) | 0.068 | 0.076 | 0.084 | V |
|  |  | Vtdac26_4W | Step 26 (Initial state+13) | 0.050 | 0.058 | 0.066 | V |
|  |  | Vtdac28_4W | Step 28 (Initial state+14) | 0.032 | 0.040 | 0.048 | V |
|  |  | Vtdac30_4W | Step 30 (Initial state+15) | 0.012 | 0.020 | 0.028 | V |

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| Parameter |  | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | min |  | typ | max |  |
| Current setting comparator threshold voltage (current step switching) | 2W1-2-phase drive (1/8-step at LV8712T) |  | Vtdac0_2W | Step 0 (When initialized: channel 1 comparator level) | 0.191 | 0.2 | 0.209 | V |
|  |  | Vtdac4_2W | Step 4 (Initial state+1) | 0.187 | 0.196 | 0.205 | V |
|  |  | Vtdac8_2W | Step 8 (Initial state+2) | 0.175 | 0.184 | 0.193 | V |
|  |  | Vtdac12_2W | Step 12 (Initial state+3) | 0.158 | 0.166 | 0.174 | V |
|  |  | Vtdac16_2W | Step 16 (Initial state+4) | 0.132 | 0.140 | 0.148 | V |
|  |  | Vtdac20_2W | Step 20 (Initial state+5) | 0.102 | 0.110 | 0.118 | V |
|  |  | Vtdac24_2W | Step 24 (Initial state+6) | 0.068 | 0.076 | 0.084 | V |
|  |  | Vtdac28_2W | Step 28 (Initial state+7) | 0.032 | 0.040 | 0.048 | V |
|  | W1-2-phase drive | Vtdac0_W | Step 0 (When initialized: channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |
|  | (quarter-step | Vtdac8_W | Step 8 (Initial state+1) | 0.175 | 0.184 | 0.193 | V |
|  | at LV8712T) | Vtdac16_W | Step 16 (Initial state+2) | 0.132 | 0.140 | 0.148 | V |
|  |  | Vtdac24_W | Step 24 (Initial state+3) | 0.068 | 0.076 | 0.084 | V |
|  | 1-2 phase drive (half-step at | Vtdac0_H | Step 0 (When initialized: channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |
|  | LV8712T/13T) | Vtdac16_H | Step 16 (Initial state+1) | 0.132 | 0.140 | 0.148 | V |
|  | 2 phase drive (full-step at LV8712T/13T) | Vtdac16_F | Step 16' (When initialized: channel 1 comparator level) | 0.191 | 0.200 | 0.209 | V |





Figure 3 Operating mode current drain (IM) vs VM Voltage


Figure 4 Operating mode current drain (Icc) vs Vcc Voltage

Figure 5 REG5 output voltage vs VM Voltage



Figure 7 Logic pin input current vs VIN Voltage


Figure 9 Output on Resistance vs Output Current(VM=12V)


Figure 11 Output on Resistance ( $\mathrm{VM}=12 \mathrm{~V}, \mathrm{Io}=0.8 \mathrm{~A}$ ) vs Temperature


Figure 10 Output on Resistance vs Output Current(VM=4V)



Figure 13 Diode forward voltage vs Diode Current


Figure 14 Output leakage voltage vs Temperature


Figure 15 Vcc low-voltage cutoff voltage vs Temperature




Figure 19 MONI pin saturation voltage vs Output current

LV8712T/LV8713T
Pin Functions

| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| $\begin{gathered} \hline 1 \\ 2 \\ 7 \\ 8 \\ 9 \\ 13 \\ 14 \\ 24 \end{gathered}$ | RST <br> OE <br> STEP <br> ATT1 <br> ATT2 <br> MD2 <br> MD1 <br> FR | Excitation reset signal input pin. <br> Output enable signal input pin. <br> STEP signal input pin. <br> Motor holding current switching pin. <br> Motor holding current switching pin. <br> Excitation mode switching pin 2. <br> Excitation mode switching pin 1. <br> CW / CCW switching signal input pin. |  |
| 4 | PS | Power save signal input pin. |  |
| 16 <br> 17 <br> 18 <br> 20 <br> 21 <br> 23 | OUT2B <br> RNF2 <br> OUT2A <br> OUT1B <br> RNF1 <br> OUT1A | Channel 2 OUTB output pin. <br> Channel 2 current-sense resistor connection pin. <br> Channel 2 OUTA output pin. <br> Channel 1 OUTB output pin. <br> Channel 1 current-sense resistor connection pin. <br> Channel 1 OUTA output pin |  |
| 6 | VREF | Constant current control reference voltage input pin. |  |

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| Pin No. | Pin Name | Pin Function | Equivalent Circuit |
| :---: | :---: | :---: | :---: |
| 3 | REG5 | Internal power supply capacitor connection pin. |  |
| 5 | MONI | Position detection monitor pin. |  |
| 10 | CHOP | Chopping frequency setting capacitor connection pin. |  |

## Operation description

## Stepping motor control

## 1. Power save function

This IC is switched between standby and operating mode by setting the PS pin. In standby mode, the IC is set to power-save mode and all logic is reset. In addition, the internal regulator circuit does not operate in standby mode.

| PS | Mode | Internal regulator |
| :---: | :---: | :---: |
| Low or Open | Standby mode | Standby |
| High | Operating mode | Operating |

## 2. The recommended order of power supply

It is recommendable that the power supplies are turned on in the following order.
VCC power supply $\rightarrow$ VM power supply $\rightarrow$ PS pin $=$ High
For turning off the power supplies, the order should be reversed.
However, the above-mentioned order is presented only as a recommendation, and noncompliance is not going to be the cause of over-current or IC destruction.

## 3. STEP pin function

| Input |  | Operating mode |
| :---: | :---: | :---: |
| PS | STP |  |
| Low | ${ }^{*}$ | Standby mode |
| High | Excitation step proceeds |  |
| High | $\square$ | Excitation step is kept |

STEP input advances electrical angle at every rising edge (advances step by step).
STEP input MIN pulse width (common in $\mathrm{H} / \mathrm{L}$ ): 500 ns (MAX input frequency: 1 MHz )
However, constant current control is performed by PWM during chopping period, which is set by the capacitor connected between CHOP and GND. You need to perform chopping more than once per step. For this reason, for the actual STEP frequency, you need to take chopping frequency and chopping count into consideration.
For example, if chopping frequency is $50 \mathrm{kHz}(20 \mu \mathrm{~s})$ and chopping is performed twice per step, the maximum STEP frequency is obtained as follows: $f=1 /(20 \mu \mathrm{~s} \times 2)=25 \mathrm{kHz}$.

## 4. Input timing



TstepH/TstepL: Clock H/L pulse width (min 500ns)
Tds: Data set-up time (min 500ns)
Tdh: Data hold time (min 500ns)
Figure 20. Input timing chart

## 5. Microstepping mode setting function (initial position)

<LV8712T>

| MD1 | MD2 | Microstepping | Excitation mode | Initial position |  |
| :---: | :---: | :--- | :--- | :---: | :---: |
|  |  | Resolution |  | Channel 1 | Channel 2 |
| Low | Low | Full Step | 2 Phase | $100 \%$ | $-100 \%$ |
| High | Low | Half Step | $1-2$ Phase | $100 \%$ | $0 \%$ |
| Low | High | Quarter Step | W1-2 Phase | $100 \%$ | $0 \%$ |
| High | High | $1 / 8$ Step | 2W1-2 Phase | $100 \%$ | $0 \%$ |

<LV8713T>

| MD1 | MD2 | Microstepping <br> Resolution | Excitation mode | Initial position |  |
| :---: | :---: | :--- | :--- | :---: | :---: |
|  |  |  |  | Channel 1 | Channel 2 |
| Low | Low | Full Step | 2 Phase | $100 \%$ | $-100 \%$ |
| High | Low | Half Step | $1-2$ Phase | $100 \%$ | $0 \%$ |
| Low | High | $1 / 16$ Step | 4W1-2 Phase | $100 \%$ | $0 \%$ |
| High | High | $1 / 32$ Step | 8W1-2 Phase | $100 \%$ | $0 \%$ |

This is the initial position of each excitation mode in the initial state after power-on and when the counter is reset.

## 6. Initial Position monitoring function

MONI pin monitors the initial position which is open drain.
When the excitation is in the initial position, the MONI output is turned on.
(Refer to " (13) Examples of current waveforms in the respective excitation modes.")
7. Reset function

| RST | Operating mode |
| :---: | :---: |
| High | Normal operation |
| Low | Reset state |



Figure 21. Reset function timing chart

When the RST pin is Low, the excitation position of the output is forcibly set to the initial position, and the MONI output is turned on. When RST turns High, the excitation position is advanced by the next STEP input.

## 8. Output enable function

| OE | Operating mode |
| :---: | :---: |
| Low | Output ON |
| High | Output OFF |



Figure 22. Output enable function timing chart
When the OE pin is High, the output turns OFF by force and turns to high impedance. However, since the internal logic circuits are under operation, the excitation position proceeds when the STEP signal is input. Therefore, when OE turns Low again, the output level follows the excitation position led by the STEP input.
9. Forward/reverse switching function

| FR | Operating mode |
| :---: | :---: |
| Low | Clockwise (CW) |
| High | Counter-clockwise (CCW) |



Figure 23. Forward/Reverse switching function timing chart
The internal D/A converter proceeds by one bit at the rising edge of the input STEP pulse. In addition, CW and CCW mode are switched by setting the FR pin.
In CW mode, the channel 2 current phase is delayed by $90^{\circ}$ relative to the channel 1 current.
In CCW mode, the channel 2 current phase is advanced by $90^{\circ}$ relative to the channel 1 current.

## 10. Constant current control setting

The setting of STM driver's constant current control is determined by the following based on the VREF voltage and the resistor connected between RNF and GND.
IOUT = (VREF/5) /RNF resistance

* The above formula gives setting value where the output current is $100 \%$ in each excitation mode.

If VREF is open or the setting is out of the recommendation operating range, output current will increase and you cannot set constant current under normal condition. Hence, make sure that VREF is set in accordance with the specification.
However, if current control is not performed (if the IC is used by saturation drive or used without current limit at DCM) make sure that the setting is as follows: $\mathrm{VREF}=5 \mathrm{~V}$ or $\mathrm{VREF}=\mathrm{VREG5}$

Power dissipation of RF resistor is obtained as follows: $\mathrm{Pd}={ }^{\text {lout }}{ }^{2} \times \mathrm{RF}$. Make sure to take allowable power dissipation into consideration when you select RF resistor.

The voltage input to the VREF pin can be switched to four-step settings depending on the statuses of the two inputs, ATT1 and ATT2. This is effective for reducing power consumption when motor holding current is supplied.
Attenuation function for VREF input voltage

| ATT1 | ATT2 | Current setting reference voltage attenuation ratio |
| :---: | :---: | :---: |
| Low | Low | $100 \%$ |
| High | Low | $80 \%$ |
| Low | High | $60 \%$ |
| High | High | $40 \%$ |

The formula is given below which is used to calculate the output current when using the function for attenuating the VREF input voltage.

IOUT $=(\mathrm{VREF} / 5) \times($ attenuation ratio $) /$ RNF resistance
Example: At VREF of 1.0 V and a reference voltage setting is $100 \%[(A T T 1, A T T 2)=(L, L)]$ and an RNF resistance of $0.5 \Omega$, the output current is set as follows.

$$
\mathrm{IOUT}=1.0 \mathrm{~V} / 5 \times 100 \% / 0.5 \Omega=400 \mathrm{~mA}
$$

If (ATT1, ATT2) is set to $(\mathrm{H}, \mathrm{H})$ in this state, IOUT is obtained as follows:
IOUT $=400 \mathrm{~mA} \times 40 \%=160 \mathrm{~mA}$
In this way, the output current is attenuated when the motor holding current is supplied for power saving.

Figure 24. Constant current control (Attenuation function) waveform
[LV8713T]
$\mathrm{VCc}=5 \mathrm{~V}, \mathrm{VM}=12 \mathrm{~V}$
VREF=1V, RNF=0.51 $\Omega$
PS=High, RST=High, ATT1=Low
MD1 $=$ MD2 $=$ High, $\mathrm{fSTEP}=10 \mathrm{kHz}$


## 11. Chopping frequency setting

For constant-current control, this IC performs chopping operations at the frequency determined by the capacitor (Cchop) connected between the CHOP pin and GND.
The chopping frequency is set as shown below by the capacitor (Cchop) connected between the CHOP pin and GND.

Tchop $\approx$ Cchop $\times$ Vtchop $\times 2$ / Ichop (s)<br>Vtchop: Width of threshold voltage (VchopH-VchopL), typ 0.5 V<br>Ichop: Charge/discharge current, typ $10 \mu \mathrm{~A}$

Fchop $\approx 1$ / Tchop (Hz)

For instance, when Cchop is 220 pF , the chopping frequency will be as follows:

$$
\text { Fchop }=1 / \text { Tchop }=10 \mu \mathrm{~A} /(220 \mathrm{pF} \times 0.5 \mathrm{~V} \times 2)=45 \mathrm{kHz}
$$

The higher the chopping frequency is, the greater the output switching loss becomes. As a result, heat generation issue arises. The lower the chopping frequency is, the lesser the heat generation becomes. However, current ripple occurs. Since noise increases when switching of chopping takes place, you need to adjust frequency with the influence to the other devices into consideration. The frequency range should be between 40 kHz and 125 kHz .

## 12. Output current vector locus (one step is normalized to 90 degrees)



Figure 25.Output current vector

Setting current ration in each Microstepping mode

| STEP | LV8713T selectable |  |  |  | LV8712T selectable |  |  |  | LV8712T/LV8713T selectable |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1/32 Step |  | 1/16 Step |  | 1/8 Step |  | Quarter Step |  | Half Step |  | Full Step |  |
|  | Ch- 1 <br> (\%) | Ch- 2 <br> (\%) | Ch- 1 <br> (\%) | Ch- 2 <br> (\%) | Ch- 1 (\%) | Ch- 2 <br> (\%) | Ch- 1 <br> (\%) | Ch- 2 <br> (\%) | Ch-1 (\%) | Ch- 2 <br> (\%) | Ch- 1 (\%) | Ch- 2 <br> (\%) |
| $\theta 0$ | 100 | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 100 | 0 |  |  |
| $\theta 1$ | 100 | 5 |  |  |  |  |  |  |  |  |  |  |
| $\theta 2$ | 100 | 10 | 100 | 10 |  |  |  |  |  |  |  |  |
| $\theta 3$ | 99 | 15 |  |  |  |  |  |  |  |  |  |  |
| $\theta 4$ | 98 | 20 | 98 | 20 | 98 | 20 |  |  |  |  |  |  |
| $\theta 5$ | 97 | 24 |  |  |  |  |  |  |  |  |  |  |
| $\theta 6$ | 96 | 29 | 96 | 29 |  |  |  |  |  |  |  |  |
| $\theta 7$ | 94 | 34 |  |  |  |  |  |  |  |  |  |  |
| $\theta 8$ | 92 | 38 | 92 | 38 | 92 | 38 | 92 | 38 |  |  |  |  |
| $\theta 9$ | 90 | 43 |  |  |  |  |  |  |  |  |  |  |
| $\theta 10$ | 88 | 47 | 88 | 47 |  |  |  |  |  |  |  |  |
| $\theta 11$ | 86 | 51 |  |  |  |  |  |  |  |  |  |  |
| $\theta 12$ | 83 | 55 | 83 | 55 | 83 | 55 |  |  |  |  |  |  |
| $\theta 13$ | 80 | 60 |  |  |  |  |  |  |  |  |  |  |
| $\theta 14$ | 77 | 63 | 77 | 63 |  |  |  |  |  |  |  |  |
| $\theta 15$ | 74 | 67 |  |  |  |  |  |  |  |  |  |  |
| $\theta 16$ | 70 | 70 | 70 | 70 | 70 | 70 | 70 | 70 | 70 | 70 | 100 | 100 |
| $\theta 17$ | 67 | 74 |  |  |  |  |  |  |  |  |  |  |
| $\theta 18$ | 63 | 77 | 63 | 77 |  |  |  |  |  |  |  |  |
| $\theta 19$ | 60 | 80 |  |  |  |  |  |  |  |  |  |  |
| $\theta 20$ | 55 | 83 | 55 | 83 | 55 | 83 |  |  |  |  |  |  |
| $\theta 21$ | 51 | 86 |  |  |  |  |  |  |  |  |  |  |
| $\theta 22$ | 47 | 88 | 47 | 88 |  |  |  |  |  |  |  |  |
| $\theta 23$ | 43 | 90 |  |  |  |  |  |  |  |  |  |  |
| $\theta 24$ | 38 | 92 | 38 | 92 | 38 | 92 | 38 | 92 |  |  |  |  |
| $\theta 25$ | 34 | 94 |  |  |  |  |  |  |  |  |  |  |
| $\theta 26$ | 29 | 96 | 29 | 96 |  |  |  |  |  |  |  |  |
| $\theta 27$ | 24 | 97 |  |  |  |  |  |  |  |  |  |  |
| $\theta 28$ | 20 | 98 | 20 | 98 | 20 | 98 |  |  |  |  |  |  |
| $\theta 29$ | 15 | 99 |  |  |  |  |  |  |  |  |  |  |
| $\theta 30$ | 10 | 100 | 10 | 100 |  |  |  |  |  |  |  |  |
| $\theta 31$ | 5 | 100 |  |  |  |  |  |  |  |  |  |  |
| $\theta 32$ | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 100 |  |  |

## 13. Typical current waveform in each excitation mode

Figure 26. Full-Step resolution (FR="Low")


Figure 27. Half-Step resolution (FR="Low")


Figure 28. Quarter-Step resolution (FR="Low") (LV8712T)


Figure 29. 1/8-Step resolution (FR="Low")
(LV8712T)


Figure 30. 1/16-Step resolution (FR="Low") (LV8713T)


Figure 31. 1/32-Step resolution (FR="Low") (LV8713T)

14. Constant Current control (Chopping operation)
(Sine wave increasing direction)

(Sine wave decreasing direction)

STEP


Figure 32. Constant current control timing chart
In each current mode, the operation sequence is as described below:

- At rise of chopping frequency, the CHARGE mode begins. (The Blanking section in which the CHARGE mode is forced regardless of the magnitude of the coil current (ICOIL) and set current (IREF) exists for $1 \mu \mathrm{~s}$.)
- The coil current (ICOIL) and set current (IREF) are compared in this blanking time.

When (ICOIL < IREF) state exists;
The CHARGE mode up to ICOIL $\geq$ IREF, then followed by changeover to the SLOW DECAY mode, and finally by the FAST DECAY mode for approximately $1 \mu \mathrm{~s}$.
When (ICOIL < IREF) state does not exist;
The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.
Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.
15. Output transistor operation


Figure 33 . Output transistor operation sequence
This IC controls constant current by performing chopping to output transistor.
As shown above, by repeating the process from 1 to 6 , setting current is maintained.
Chopping consists of 3 modes: Charge/ Slow decay/ Fast decay. In this IC, for switching mode (No.2, 4, 6), there are "off period" in upper and lower transistor to prevent crossover current between the transistors. This off period is set to be constant ( $\approx 0.375 \mu \mathrm{~s}$ ) which is controlled by the internal logic. The diagrams show parasitic diode generated due to structure of MOS transistor. When the transistor is off, output current is regenerated through this parasitic diode.

Output FET control function
OUTA $\rightarrow$ OUTB (CHARGE)

| Output Tr | CHARGE | SLOW | FAST |
| :---: | :---: | :---: | :---: |
| U1 | ON | OFF | OFF |
| U2 | OFF | OFF | ON |
| L1 | OFF | ON | ON |
| L2 | ON | ON | OFF |
| Output Tr CHARGE SLOW FAST <br> U1 OFF OFF ON <br> U2 ON OFF OFF <br> L1 ON ON OFF <br> L2 OFF ON ON |  |  |  | | OUTBAR |
| :--- |

Figure 34.Constant current control waveform [LV8713T]
$\mathrm{Vcc}=5 \mathrm{~V}$, $\mathrm{VM}=12 \mathrm{~V}$
VREF $=1 \mathrm{~V}, \mathrm{RNF}=0.51 \Omega$, Cchop $=220 \mathrm{pF}$ PS=High, RST=High, ATT1=ATT2=Low MD1=High, MD2=Low, fSTEP=100Hz


Figure 35. Constant current control waveform (Stationary state)

Motor current switches to Fast Decay mode when triangle wave (CHOP) switches from Discharge to Charge. Approximately after $1 \mu \mathrm{~s}$, the motor current switches to Charge mode. When the current reaches to the setting current, it is switched to Slow Decay mode which continues over the Discharge period of triangle wave.


Figure 36. Constant current control waveform (Increasing direction)


Figure 37. Constant current control waveform (Decreasing direction)

## 16. Blanking time

If, when exercising PWM constant-current chopping control over the motor current, the mode is switched from decay to charge, the recovery current of the parasitic diode may flow to the current sensing resistance, causing noise to be carried on the current sensing resistance pin, and this may result in false over current detection. To prevent this false detection, a blanking time is provided to prevent the noise occurring during mode switching from being received. During this time, the mode is not switched from charge to decay even if noise is carried on the current sensing resistance pin.
The blanking time, tBLANK ( $\mu \mathrm{s}$ ), is approximately

$$
\mathrm{tBLANK} \approx 1 \mu \mathrm{~s}
$$

Figure 38. Blanking time waveform [LV8713T]

Vcc=5V, VM=12V
$\mathrm{VREF}=5 \mathrm{~V}, \mathrm{RNF}=1 \mathrm{~V}, \mathrm{CCHOP}=220 \mathrm{pF}$ PS=High,


From the above Fig. , the blanking time appears to be $1.5 \mu \mathrm{~s}$. However, since the mode shifts from charge (blanking time), OFF, to DECAY, the actual blanking time is obtained as follows:
Blanking time $=1 \mu \mathrm{~s}+$ OFF zone $=0.5 \mu \mathrm{~s}$

## 17. Microstepping mode switching operation

When Microstepping mode is switched while the motor is rotating, each drive mode operates with the following sequence.

FR="Low"

*As for $\theta 0$ to $\theta 32$, please refer to the step position of current ratio setting.

If you switch Microstepping mode while the motor is driving, the mode setting will be reflected from the next STEP and the motor advances to the position shown in the following.
(a) Microstepping (1/32-,1/16-,1/8-,Quarter-.Half-step) $\rightarrow$ Microstepping (1/32-,1/16-, $1 / 8-$-Quarter-.Half-step)

When a microstepping switches to the next microstepping, the excitation position is switched to the next corresponding step angle of the next microstepping mode.
e.g.) When the rotation direction is forward at $1 / 16$-step ( $\theta 6$ ) and if you switch to $1 / 8$ step, the step angle is set to $\theta 8$ at the next step.
When the rotation direction is forward at $1 / 16$-step ( $\theta 20$ ) and if you switch to $1 / 8$ step, the step angle is set to $\theta 24$ at the next step.
(b) Microstepping (1/32-, 1/16-, 1/8-,Quarter-.Half-step) $\rightarrow$ Full-step

When a microstepping switches to the full-step, the excitation position is switched to full-step angle of the present quadrant. Caution is required when switching from $\theta 16$ or higher step angle of microstepping position to full-step.
e.g.) When the rotation direction is forward at $1 / 8$ step ( $\theta 8$ ) and if you switch to full-step, the step angle is set to $\theta 16$ ' at the next step.
When the rotation direction is forward at $1 / 8$ step ( $\theta 16$ ) and if you switch to full-step, the step angle is set to $\theta 16$ ' at the next step. (the electric angle is the same but the absolute value changes)
When the rotation direction is forward at $1 / 8$ step ( $\theta 24$ ) (the electric angle returns and the absolute value changes)
(c) Full-step $\rightarrow$ Microstepping (1/32-,1/16-, 1/8-,Quarter-.Half-step)

When full step switches to microstepping, the excitation position is switched to the next corresponding step angle.
e.g.) When the rotation direction is forward at Full step ( $\theta 16^{\prime}$ ) and if you switch to $1 / 8$ step, the step angle is set to $\theta 20$ at the next step.

```
Microstep mode switching operation
[LV8712T]
Vcc=5V, VM=12V
VREF=1V,RNF=0.51 \Omega
PS=High, RST=High, fSTEP=100Hz
```

Figure 39
Microstepping ( $1 / 8$ step) $\rightarrow$ Microstepping (quarter step)


Figure 40.
Microstepping (Half-step) $\rightarrow$ Microstepping ( $1 / 8$ step)

Figure 41
Microstepping (quarter step) $\rightarrow$ Full step MD1=Low


Figure 42.
Full step $\rightarrow$ Microstepping (quarter step)


## Thermal shutdown function

The thermal shutdown circuit is incorporated and the output is turned off when junction temperature Tj exceeds $180^{\circ} \mathrm{C}$. As the temperature falls by hysteresis, the output turned on again (automatic restoration). The thermal shutdown circuit does not guarantee the protection of the final product because it operates when the temperature exceed the junction temperature of Tjmax $=150^{\circ} \mathrm{C}$.

$$
\begin{aligned}
& \mathrm{TSD}=180^{\circ} \mathrm{C} \text { (typ) } \\
& \Delta \mathrm{TSD}=40^{\circ} \mathrm{C} \text { (typ) }
\end{aligned}
$$

## Application Circuit Example



The formulae for setting the constants in the examples of the application circuits above are as follows:
Constant current (100\%) setting
When VREF $=1.0 \mathrm{~V}$

$$
\begin{aligned}
\text { IOUT } & =\text { VREF/5/RNF resistance } \\
& =1.0 \mathrm{~V} / 5 / 0.47 \Omega=0.426 \mathrm{~A}
\end{aligned}
$$

Chopping frequency setting
Fchop $=$ Ichop/ $($ Cchop $\times$ Vtchop $\times 2)$

$$
=10 \mu \mathrm{~A} /(180 \mathrm{pF} \times 0.5 \mathrm{~V} \times 2)=55 \mathrm{kHz}
$$

## Allowable power dissipation

## Evaluation board

Size: $57 \mathrm{~mm} \times 57 \mathrm{~mm} \times 1.7 \mathrm{~mm}$, glass epoxy 2-layer board


## Evaluation board Design Diagram




TOP View

## Evaluation board

1. Completed PCB with Devices

The evaluation board of LV8712T and LV8713T is common.

PCB size: $57 \mathrm{~mm} \times 57 \mathrm{~mm} \times 1.7 \mathrm{~mm}$, glass epoxy 2-layer board

2.Bill of Materials for LV8712T/13T Evaluation Board

| Designator | Quantity | Description | Value | Tolerance | Footprint | Manufacturer | Manufacturer Part Number | Substitution Allowed | Lead Free |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | 1 | REG5 stabilization Capacitor | $\begin{aligned} & 0.1 \mu \mathrm{~F}, \\ & 100 \mathrm{~V} \end{aligned}$ | $\pm 10 \%$ |  | Murata | GRM188R72A104KA35* | Yes | Yes |
| C2 | 1 | ```Capacitor to set chopping frequency``` | $\begin{gathered} 180 \mathrm{pF}, \\ 50 \mathrm{~V} \end{gathered}$ | $\pm 5 \%$ |  | Murata | GRM1882C1H181JA01* | Yes | Yes |
| C3 | 1 | VCC Bypass Capacitor | $\begin{gathered} 0.1 \mu \mathrm{~F}, \\ 100 \mathrm{~V} \\ \hline \end{gathered}$ | $\pm 10 \%$ |  | Murata | GRM188R72A104KA35* | Yes | Yes |
| C4 | 1 | VM Bypass Capacitor | $10 \mu \mathrm{~F}$, 50 V | $\pm 20 \%$ |  | SUN Electronic Industries | 50ME10HC | Yes | Yes |
| R1 | 1 | Pull-up Resistor for for pin MONI | $\begin{aligned} & 47 \mathrm{k} \Omega, \\ & 1 / 10 \mathrm{~W} \end{aligned}$ | $\pm 5 \%$ |  | KOA | RK73B1JT**473J | Yes | Yes |
| R2 | 1 | Channel 1 output current detective Resistor | $\begin{gathered} 0.47 \Omega, \\ 1 \mathrm{~W} \end{gathered}$ | $\pm 5 \%$ |  | ROHM | MCR100JZHJLR47 | Yes | Yes |
| R3 | 1 | Channel 2 <br> output current <br> detective <br> Resistor | $\begin{gathered} 0.47 \Omega, \\ 1 \mathrm{~W} \\ \hline \end{gathered}$ | $\pm 5 \%$ |  | ROHM | MCR100JZHJLR47 | Yes | Yes |
|  |  |  |  |  |  |  | LV8712T |  |  |
| IC1 | 1 | Motor Driver |  |  | (225mil) | semiconductor | LV8713T | No | Yes |
| SW1-SW8 | 8 | Switch |  |  |  | MIYAMA ELECTRIC | MS-621C-A01 | Yes | Yes |
| TP1-TP21 | 21 | Test Point |  |  |  | MAC8 | ST-1-3 | Yes | Yes |

## 3.Evaluation board circuit



## 4.Evaluation Board Manual

| [Supply Voltage] | VM $(4$ to 16 V$):$ Motor Power Supply <br>  <br>  <br>  <br> VCC (2.7 to 5.5 V$):$ Control Power Supply <br> VREF (0 to VCC-1.8V): Const. Current Control for Reference Voltage |
| :--- | :--- |
| [Toggle Switch State] | Upper Side: High (VCC) <br> Middle: Open, enable to external logic input <br> Lower Side: Low (GND) |

[Operation Guide]

1. Initial Condition Setting: Set "Open or Low" all switches
2. Motor Connection: Connect the Motors between OUT1A and OUT1B, between OUT2A and OUT2B.
3. Power Supply: Supply DC voltage to VCC, VM and VREF.
4. Ready for Operation from Standby State: Turn "High" the PS pin toggle switch. Channel 1 and 2 are into full-step excitement initial position ( $100 \%,-100 \%$ ) .
5. Motor Operation: Turn "High" the RST pin toggle switch. Input the clock signal into the pin STEP.
6. Other Setting (See Application Note for detail)
i. ATT1, ATT2: Motor current attenuation.
ii. FR: Motor rotation direction (CW / CCW) setting.
iii. MD1, MD2: Microstepping Resolution.
iv. OE: Output Enable.
[Setting for External Component Value]
7. Constant Current (100\%)

$$
\begin{aligned}
\text { At VREF } & =1.0 \mathrm{~V} \\
\text { lout } & =V R E F[\mathrm{~V}] / 5 / \mathrm{RNF}[\mathrm{ohm}] \\
& =1.0[\mathrm{~V}] / 5 / 0.47[\mathrm{ohm}] \\
& =0.426[\mathrm{~A}]
\end{aligned}
$$

2. Chopping Frequency

Fchop $=$ Ichop $[\mathrm{LA}] /($ Cchop $\times$ Vt $\times 2)$

$$
\begin{aligned}
& =10[\mathrm{uA}] /(180[\mathrm{pF}] \times 0.5[\mathrm{~V}] \times 2) \\
& =55[\mathrm{kHz}]
\end{aligned}
$$

## 5. Evaluation Board waveform (Stepping motor drive)

```
LV8712T
    VM=12V,VCC=5V,VREF=1.0V
    PS=High,RST=High
    ATT1=ATT2=FR=OE=Low
```

Figure 43.
Full-step (MD1=MD2=Low, fSTEP=500Hz)


Figure 44.
Half-step (MD1=High, MD2=Low, fSTEP=1 kHz)


Figure 45.
Quarter-step (MD1=Low,MD2=High, fSTEP=2kHz)


```
LV8713T
    VM=12V, VCC=5V, VREF=1.0V
    PS=High, RST=High
    ATT1=ATT2=FR=OE=Low
```

Figure 47.
Full-step (MD1=MD2=Low, fSTEP=500Hz)


Figure 49.
1/16-step (MD1=Low,MD2=High, fSTEP=8kHz)


Figure 46.
1/8-step (MD1=MD2=High, fSTEP=4kHz)


Figure 48
Half-step (MD1=High, MD2=Low, fSTEP=1 kHz)


Figure 50.
1/32-step (MD1=MD2=High, fSTEP=16kHz)


## Cautions for layout：

－Power supply connection pin 【VM】
$\checkmark$ VCC is a control power supply，and VM is a motor power supply．
$\checkmark \quad$ Make sure that supply voltage does not exceed the absolute MAX ratings under no circumstance． Noncompliance can be the cause of IC destruction and degradation．
$\checkmark \quad$ Caution is required for VM supply voltage because this IC performs switching．
$\checkmark$ The bypass capacitor of the VM power supply should be close to the IC as much as possible to stabilize voltage．Also if you intend to use high current or back EMF is high，please augment enough capacitance．

## －GND pin【GND，PGND，RNF－resistor GND line】

$\checkmark$ High current flows into the PGND and GND side of RNF resistor；therefore，connect PGND and RNF －GND independently．
$\checkmark$ On the other hand，since PGND and GND are connected through silicon board，if the line of PGND is too long，difference of electric potential occurs between PGND and GND which creates gradient to the GND electric potential within the IC board．This can be the cause of the IC malfunction．Hence make sure to connect PGND and RNF－GND independently so that the pins do not share the common impedance with GND．And GND，PGND，and RNF should be single－point grounded to the low impedance GND area near the IC．Also the capacitor between VM and GND should be connected adjacent to the IC．
－Internal power supply regulator pin 【REG5】
$\checkmark \quad$ REG5 is a power supply to drive output FET（typ 5V）．
$\checkmark$ When VM supply is powered and PS is＂High＂，REG5 operates．
$\checkmark \quad$ Please connect capacitor for stabilize REG5．The recommendation value is 0.1 uF ．
$\checkmark$ Since the voltage of REG5 fluctuates（ $\pm 10 \%$ ），do not use it as reference voltage that requires accuracy．

## －Input pin

$\checkmark$ The logic input pin incorporates pull－down resistor（100k $\Omega$ ）．
$\checkmark \quad$ When you set input pin to low voltage，please short it to GND because the input pin is vulnerable to noise．
$\checkmark \quad$ The input is TTL level（H： 2 V or higher， $\mathrm{L}: 0.8 \mathrm{~V}$ or lower）．
$\checkmark \quad$ VREF pin is high impedance．

## －OUT pin【OUT1A，OUT1B，OUT2A，OUT2B】

$\checkmark$ During chopping operation，the output voltage becomes equivalent to VM voltage，which can be the cause of noise．Caution is required for the pattern layout of output pin．
$\checkmark$ The layout should be low impedance because driving current of motor flows into the output pin．
$\checkmark$ Output voltage may boost due to back EMF．Make sure that the voltage does not exceed the absolute MAX ratings under no circumstance．Noncompliance can be the cause of IC destruction and degradation．

## －Current sense resistor connection pin【RNF1，RNF2】

$\checkmark$ To perform constant current control，please connect resistor to RNF pin．
$\checkmark$ To perform saturation drive（without constant current control），please connect RNF pin to GND．
$\checkmark$ If RNF pin is open，you cannot set constant current under normal condition．Therefore，please connect it to resistor or GND．
$\checkmark$ The motor current flows into RNF－GND line．Therefore，please connect it to common GND line and low impedance line．

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